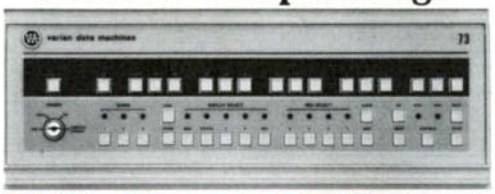
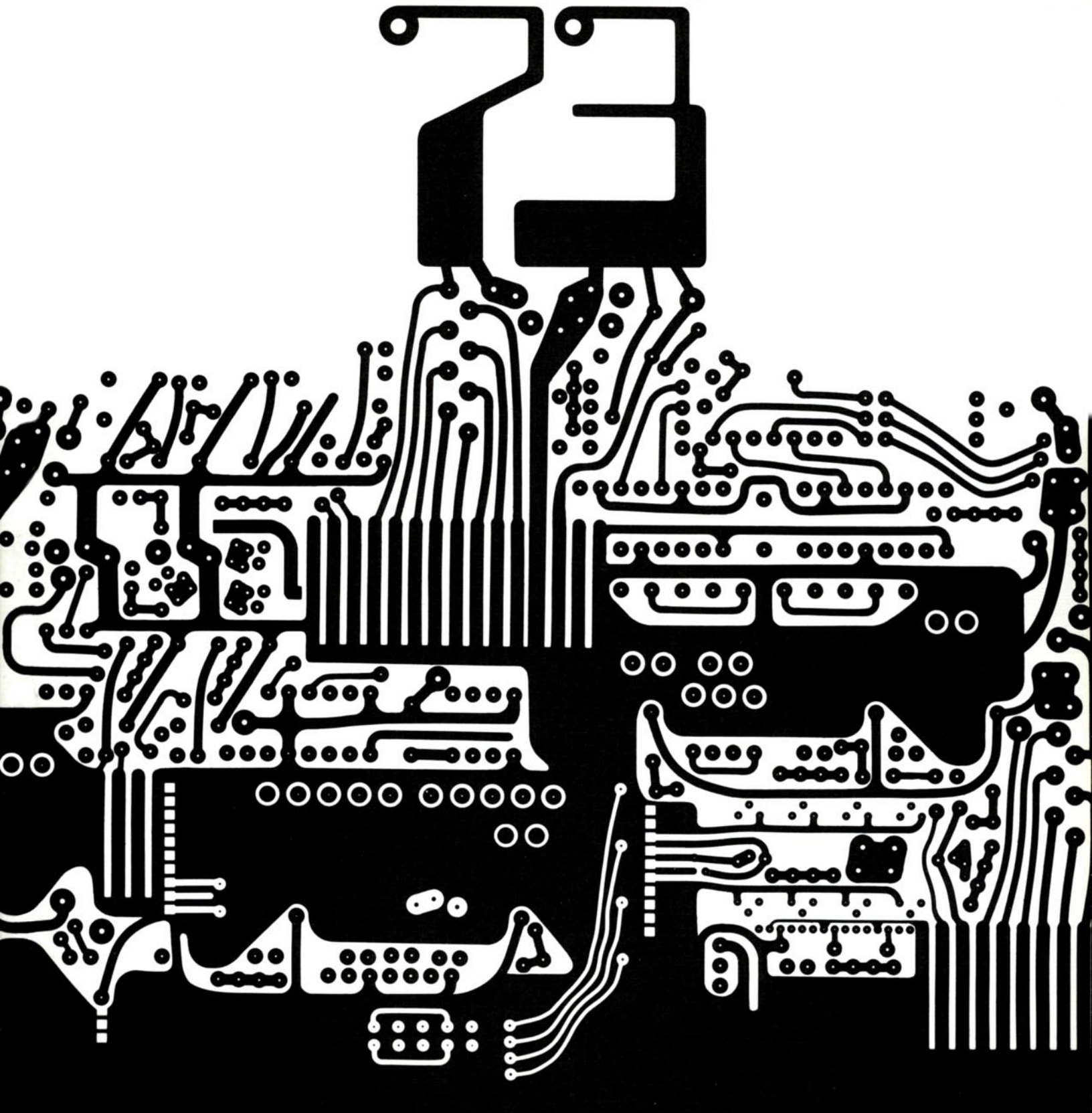
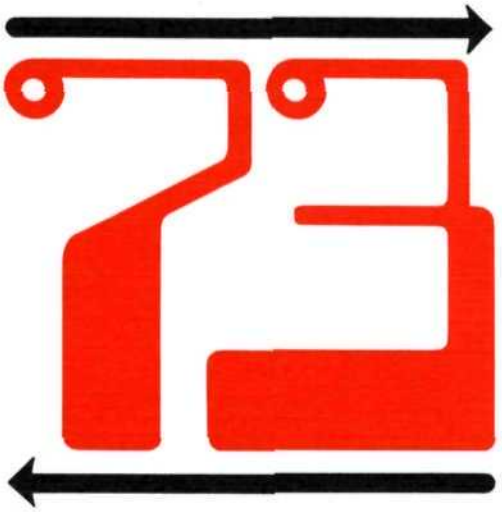
The all-new computer for
the new computer age



VARIAN





VARIAN 73 THE ALL-NEW COMPUTER FOR THE NEW COMPUTER AGE

For the better part of a decade, Varian 620-series computers have paced the minicomputer industry. Each new model has represented a dramatic improvement in performance, and an equally dramatic reduction in the dollars paid for that performance.

Now, with the introduction of the Varian 73, Varian Data Machines has achieved a major step-function change in the power and potential of the minicomputer as a systems component.

The Varian 73 has been designed specifically to meet the new, more sophisticated demands that have developed as users have gained experience in applying minicomputers to thousands of applications.

These demands have included faster processing times, a more efficient and flexible instruction repertoire, expanded memories, a faster, more versatile input/output structure, simpler interfacing between multiple processors and memories.

The Varian 73 meets all these requirements, with performance to spare.

User-Accessible Microprogramming

The Varian 73 is a microprogrammed computer, with 64-bit control words dictating the flow of data through a 16-register processing section. This powerful combination permits the writing of exceptionally fast and efficient programs. The computer can process all previous Varian 620 programs, and with the addition of a Writable Control Store option, the microprogram can be extended to meet any special system requirements.

Extendable Architecture

The Varian 73 is available with either semiconductor or core memories, or any combination of the two. With memory mapping (a future option) up to 262K of memory can be included in the system. All memories are dual port for fast interleaving of I/O and processor functions. Built-in features allow multiple central processors to share memory, greatly simplifying the implementation of a multi-processor system.

165-Nanosecond Microinstruction Time

The Varian 73 has set a new standard for processing speed. Microinstructions are carried out in 165 nanoseconds. With semiconductor memory register-reference instructions are

completed in 330 nanoseconds, memory-reference instructions in 660 nanoseconds. Cycle time for semiconductor memory modules is 330 nanoseconds: Cycle time for the core memory is 660 nanoseconds. Direct I/O-to-memory data transfers can take place at rates 0 to 3.03 million words per second.

Four Input/Output Techniques

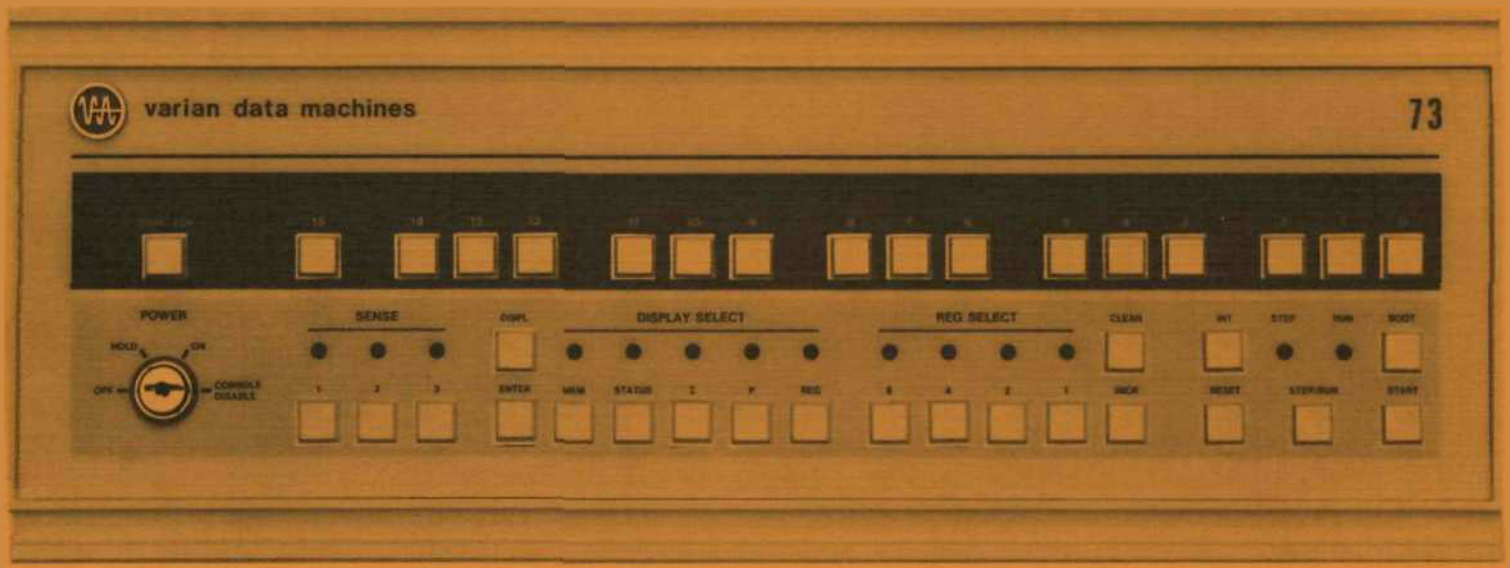
the designer and programmer have a choice of up to four different input/output techniques, depending on the data rate required and the number of peripherals on the interface. Dual-port memories allow for highly efficient direct-to-memory transfers.

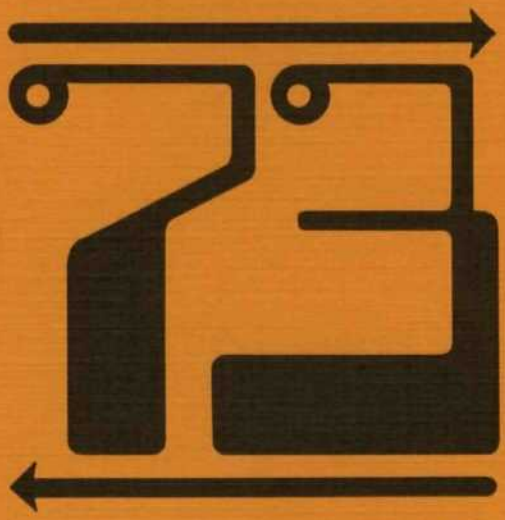
Off-The-Shelf Software and Peripherals

The Varian 73 is an all-new computer, but it is fully supported with the extensive software and peripheral interfaces that have been developed for Varian 620-series computers. Immediately available are powerful operating-system software packages such as VORTEX and MOS. Varian 73 software also includes DAS macro-assemblers for programs written in Varian 620 language, higher level language compilers such as FORTRAN IV, BASIC, and RPG IV. mathematical and data-conversion packages, and editing. debugging, and diagnostic programs.

Compact, Reliable Packaging

The entire Varian central processor, including the microprogram read-only memory, is contained on a single circuit board, 15.6 inches by 19 inches. Similar boards carry up to 8K of semiconductor or core memory. All boards plug into universal slots in either a 7-inch or a 14-inch chassis. A single power supply will accommodate systems with up to 32K of core memory. Two types of consoles are available: a programmer's console with a full set of controls and indicators, and an operator's console with just the switches needed to start, stop, and control the program.





THE ALL-NEW VARIAN 73 ... USER-ACCESSIBLE MICROPROGRAMMING FOR SPEED AND FLEXIBILITY

The Varian 73 has set a new standard for speed and flexibility.

Data flow is controlled by hundreds of microinstructions stored in a read-only memory. Execution time per microinstruction is only 165 nanoseconds. And if that isn't enough speed and flexibility, the user can add an optional Writable Control Slore to create his own microinstruction set.

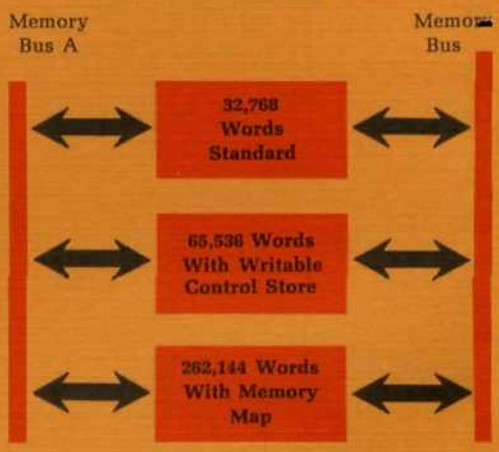
Processor Microprogram — The standard Varian 73 microprogram consists of 512 microinstructions, each a 64-bit word stored in the processor ROM. The 64 bits are divided into fields which control the flow and manipulation of data throughout the machine. A single microinstruction can dictate a number of different machine functions: register, memory and I/O transfers, arithmetic and logical operations, and tests on the conditions of registers.

User-Written Microprogram — The processor microprogram can be supplemented by an optional Writable Control Store memory containing microinstructions written by the user. The standard Varian 73 microprogram is designed to decode and emulate the widely used Varian 620 instruction set. Special microprograms can also be written, using the powerful 64-bit microinstruction format, to adapt the Varian 73 to special application requirements.

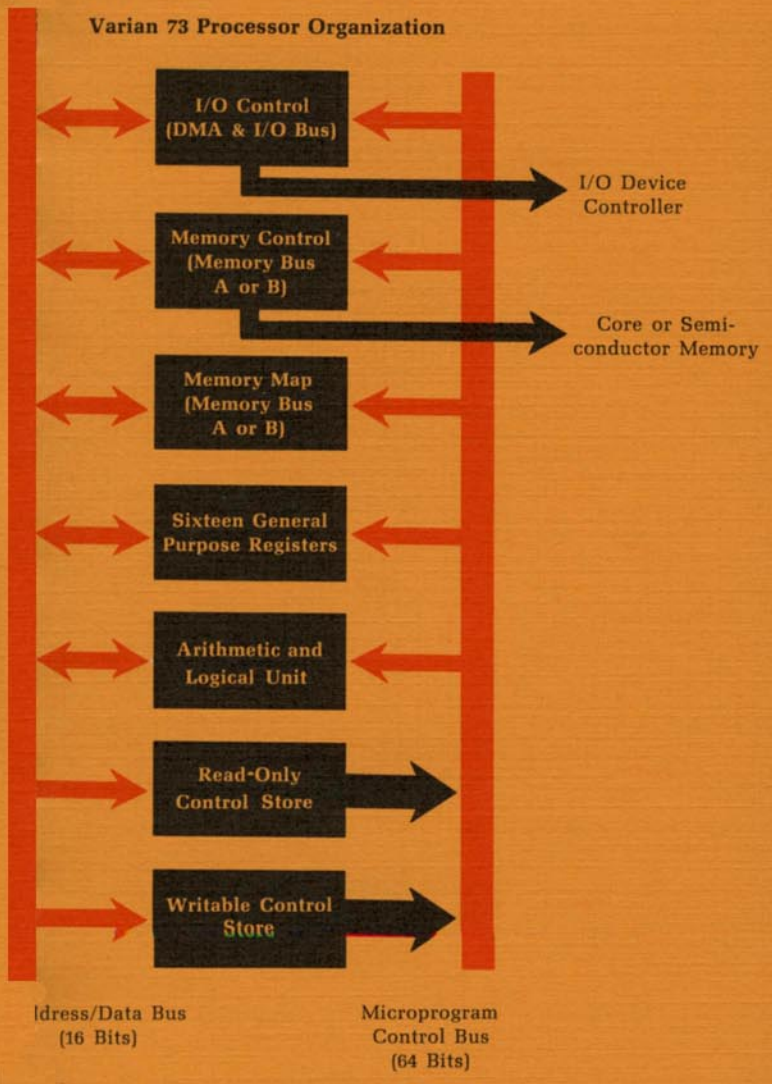
Sixteen General-Purpose Registers — Further programming flexibility is provided by 16 general-purpose and 8 special-purpose 16-bit registers, all accessible to the microprogram.

Dual Memory Buses — Processors memories, and PMA (Priority Memory Access) I/O controllers are all con nected to a common bus structure for fast data transfers and ease of expansion. Two parallel buses are provided allowing data transfer from a peripheral to a 4K or 8K memory module, for example, while the processor accesses a second memory module. Multiple processors, peripheral devices, and up to 262K words of memory can share the parallel buses. Advantages of this unique structure are detailed on the following pages.

Varian 73 Memory Expansion



Varian 73 Processor Organization



THE ALL-NEW VARIAN 73 … DUALPORT MEMORIES, CORE AND MOS, IN AN EXTENDABLE ARCHITECTURE

The Varian 73 has added a new dimension to the architecture of computer memory systems.

Both core and MOS memories are available in 8K modules, each packaged on a single board- All share a common, dual bus structure, along with multiple processors and PMA controllers. Processors equipped with the Memory Map option will be able to address 262K of memory.

Core Memories — Cycle time for core memories is a fast 660 nanoseconds. The memories are available in 4K and 8K modules.

MOS Memories — Semiconductor memories, with a cycle time of 330 nanoseconds, are available in IK, 2K, 4K. and 8K modules. They may be combined with core memories in any proportion. Addressing and programming are identical for the two types of memories. MOS memories are for optimum speed and throughput; core memories for optimum economy. A battery-powered Data Save option may be added to the power supply when semi-conductor memory is included in the system.

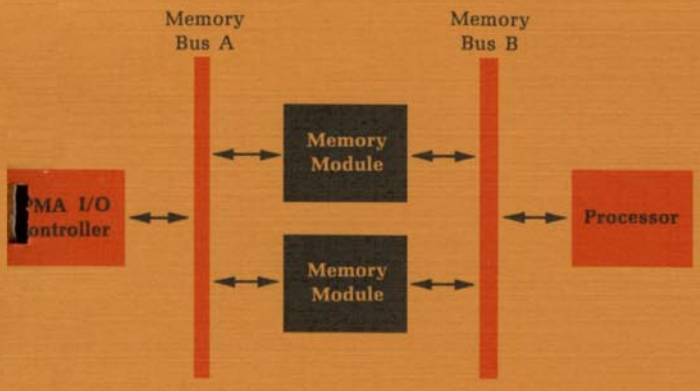
Dual Ports — Both core and MOS memories are provided with two fully implemented ports, each connected to one of two parallel memory buses. In multiple-memory systems, this means that one memory may be communicating with a processor while another is transferring data to or from another processor or an I/O device. Prioritie between the buses are implemented by memory-control circuits in response to program instructions.

Memory Mapping — The Memory Ma option performs address relocation and memory protection for up to 262K memory locations by translating the 15 bit virtual memory address and a 4-bit key into an 18-bit physical address Up to 16 independent protection partitions may be simultaneously assigned Any user program may employ up to 32K words of memory in 512-word blocks. Completely protected, read only, and common memory blocks may be defined.

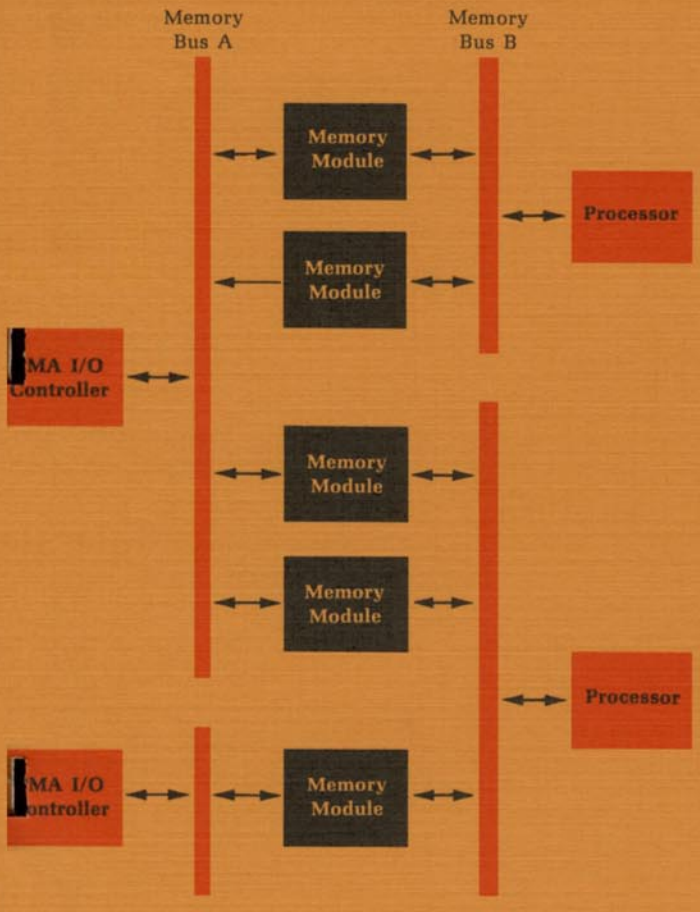
Memory Protect — The memory-protect option prevents the program from accessing any 512-word segment of memory that has been "protected" by a mask stored in the option. The 64-bit mask provides protection for a full 32K memory block. The mask can be applied, removed, and changed under program control.

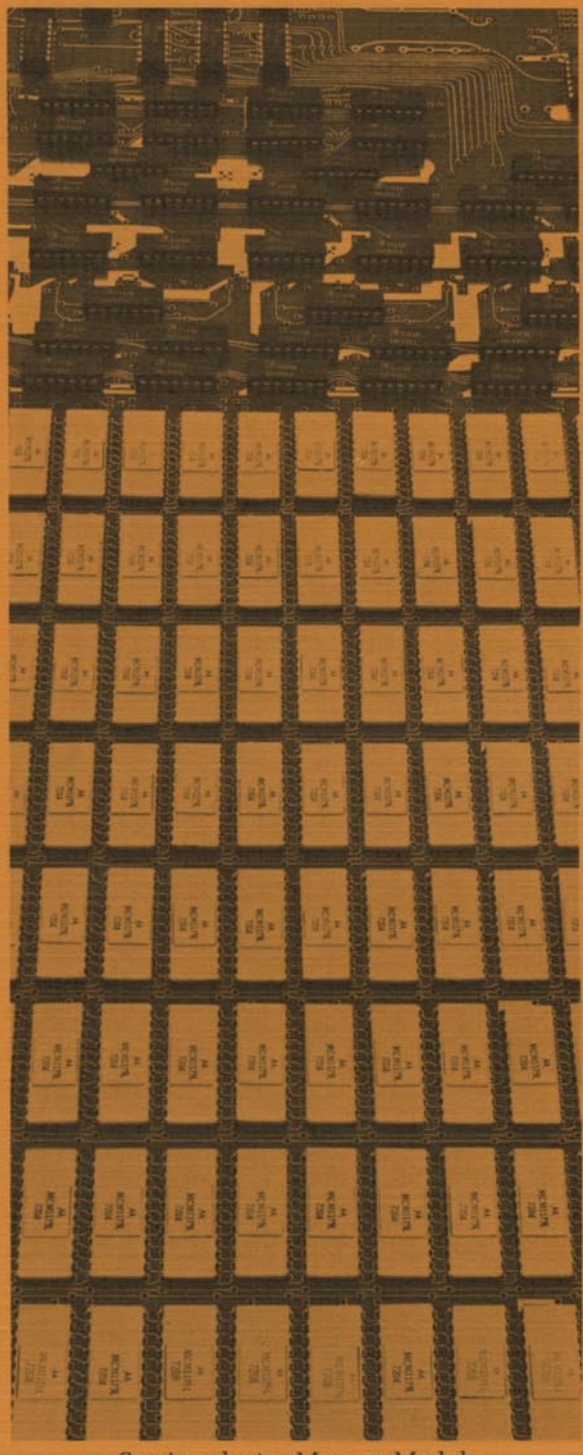
Memory Parity — Another memory option checks the parity of every data transfer on the dual memory bus. Two parity bits are used, one for the B most significant bits, the other for the 8 least significant bits. This facilitates byte packing and retrieval with a paritiy check on each byte that is transferred

Single Processor System



Dual Processor System





Semiconductor Memory Module

THE ALL-NEW VARIAN 73... FOUR WAYS TO COMMUNICATE WITH PERIPHERALS

The Varian 73 gives the system designer four different ways to communicate with peripherals and other data sources. The result is unprecedented flexibility in selecting the I/O technique that will provide the highest possible data transfer rate at minimum cost in processor time.

All data transfers, except PMA, are over the party-tine I/O bus, with 16 bi-directional lines for addresses and for data, plus an additional 14 lines for timing, sense, and control signals. PMA transfers are direct to memory, with separate 16-line buses for addresses and data.

Priority Interrupt Structure — The Varian 73 has a true hardware priority interrupt structure, expandable at low cost to up to 64 levels, with automatic interrupt identification. External controllers can all request interrupts and specify the interrupt location via the address lines of the Varian 73 I/O bus. An optional Priority Interrupt Module (PIM) provides hardware priority arbitration and interrupt address (vector) generation for 8 levels. Up to 8 PIM's may be interfaced to the I/O bus of a Varian 73 processor. Interrupts may be enabled or disabled individually or in groups.

Programmed I/O — Programmed I/O operations are initiated by the central processor and are used primarily to control and sense the state of peripherals, to prepare controllers for other types of I/O transfers, and to communicate with low-speed devices, such as a teletype. Any peripheral control! can also initiate a data transfer [or signal its completion] by an interrupt to the processor.

Direct Memory Access **(DMA)** I/O- Direct data transfers between I/O bus and memory are effected in the DMA mode. The technique is implemented by a Buffer Interlace Controller (BIC) option that stores the initial and final addresses of the data words to be transferred. The transfers are made on a "cycle stealing" basis. DMA transfers can occur at rates up to 333,000 words per second.

High-Speed DMA — Special control lines are provided for peripheral controllers that are able to operate at "high speed" DMA rates, up to 1 million words per second. A similar BIC option is used to implement transfers this higher rate.

Priority Memory Access (PMA) I/O - Data transfers at the full memory cycly rate (3.03 million words per second, in the case of a MOS memory] can be obtained through the PMA channel. PMA controller is loaded with the initial and final addresses of the data words to be transferred. Controller data and address lines are connected directly to the memory bus.

VARIAN 73 PERIPHERALS

Peripheral devices and I/O interfaces for Varian 73 systems have been field tested in hundreds of installations and have been selected to provide an optimum combination of economy and high performance.

Each standard peripheral subsystem is an integrated unit, including the device itself, interconnecting cables, I/O controller, and software for its operation. The standard Varian peripherals are supplemented by a list of over 100 other peripheral models and types that may be supplied on special order.

FXED HEAD DISCS — Low-cost storage, with capacity of 30K, 61K or 123K words; 17 ms average access time; 33.3K word transfer rate; 1 head per track.

MOVING HEAD DISCS — Capacities from 1.17 million words to 58 million words; 12.5 ms and 20 ms an-track access time, average access times to a track of 45 and 60 ms; transfer rates up to 156K words per second.

DRUM MEMORIES—Capacity of 30K, 61K, 123K, 246K, 491K. or 983K words; 7 ms average access time; 106K word transfer rate; 1 head per track.

MAGNETIC TAPE —9-track or 7-track, with up to 4 transports per controller, densities of 200, 556, and 800 bpi and speed of 25 ips.

TELETYPES—Model ASR 33, ASR 35. or KSR 35 units.

HIGH-SPEED PAPER TAPE —Punch rates up to 75 characters per second and read rates up to 300 characters per second.

CARD READER — Reading speed of 300 cards per minute.

CARD PUNCH —Punching speed of 35 cards per minute.

LINE PRINTER — 245 to 1100 lines per minute, up to 132 characters per line, buffered. ASCII code, 64 alphanumeric characters and symbols.

DIGITAL PLOTTER —300 steps per second, 0.01-inch step size, other sizes are available.

ELECTROSTATIC PLOTTER—Statos Printer/Plotters; produce graphic displays and alphanumeric information at rates up to 5,000 lines per minute.

ANALOG INPUT — Multiplex/Controllers expandable up to 256 single ended or differential channels. Analog-to-digital converters for word lengths to 13 bits, conversion rates to 55K words per second.

ANALOG OUTPUT —Controllers expandable to 64 channels, word lengths to 14 bits per channel.

DIGITAL INPUT—Multiplex/controllers expandable up to 2048 channels of 16 bits.

DIGITAL OUTPUT —Controllers expandable up to 64 output channels of 16 bits each.

CRT DISPLAY —11-inch storage scope.

RELAY INTERFACES —Contact inputs and mercury-wetted contact outputs; 0.5 to 3 A; up to 400 V.

GENERAL PURPOSE INTERFACES—Buffer Interlace Controller; Buffered I/O Controller; Digital I/O Controller; Universal Serial Asynchronous Controller.

DATA SET COUPLERS — Interface with Type 103, 201, 202 and 301 modems, hardware or software sync character detection; transmission rates up to 50,000 baud; controller available for 801 Automatic Call Unit.

COMMUNICATIONS CONTROLLER — Multiplexes, controls and provides data interface for up to 64 data sets; synchronous and asynchronous lines may be intermixed; modular line controllers for RS 232B, CCITT, discrete, and relay communication systems.

THE ALL-NEW VARIAN 73 ... POWERFUL OPERATING SYSTEMS AND SYSTEM SOFTWARE

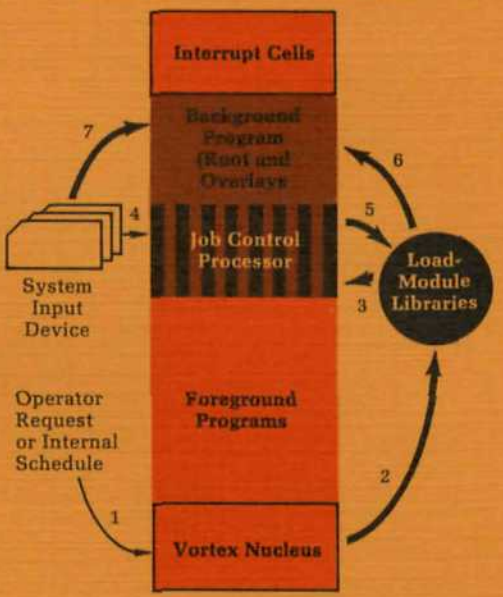
Operating Systems — Two comprehensive software operating systems are available for use with Varian 73 computers: VORTEX and MOS.

Both systems incorporate a full repertoire of utility programs, as well as DAS MR and FORTRAN IV language processors. MOS also includes RPG IV.

VORTEX [Varian Omnitask Real-Time Executive] is a multi-programming system with special features designed for real-time applications. A number of different tasks may be stored in the main memory or on a rotating memory device. These tasks are scheduled by a resident executive program that gives highest priority to real-time "foreground" programs. Lower priority "background" programs are executed during the idle-time intervals embedded in most real-time operations. The effect is to give the system the utility of two computers for the price of one.

VORTEX also increases the efficiency of any installation in which the computer is required to operate on a number of different programs in sequence. The user simply establishes the priority of the jobs to be executed; the system automatically schedules and runs the programs without further operator intervention.

Example of VORTEX Operation



When Real-Time Executive senses (1) that time is available for the scheduling of a background task [following an initial operator request], the Job Control Processor is read into the background area of the main memory [2 and 3]. The JCP responds to a directive from the System Input Device [4] and loads a background task from either the rotating memory [5 and 6] or the System Input Device [7].

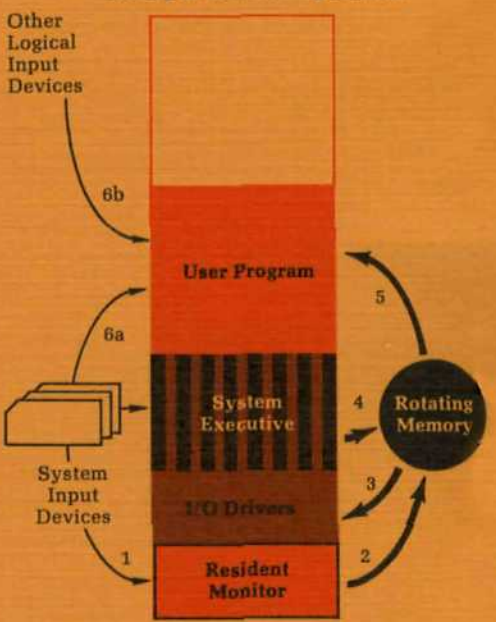
Varian **MOS** [Master Operating System) is an integrated batch-process software system designed to boost performance and simplify operation for the medium-to-large-scale system user.

MOS is available in disc, drum, and magnetic-tape resident versions, and includes a complete I/O Control System and System Executive.

Features offered by MOS are automatic identification of both printed listings and binary object output with the job title and date to provide for program control and job accountability; a system preparation program, system maintenance program, source program editor, object program debug package, and a program library.

MOS conserves main memory space for the user by allowing all software elements, except for a small Resident Monitor, to be stored on the rotating memory or magnetic tape and loaded into the computer only when needed. This applies even to the System Executive which serves as the central control element.

Example of MOS Operation



A directive from the System Input Device (1) instructs the Resident Monitor to load the System Executive, I/O Control Module, and appropriate I/O drivers (2 and 3). The System Executive loads and executes a program from the rotating memory (4 and 5) or any logical input unit (6). Programs can overlay the System Executive, but not the I/O Control and Driver modules.

SYSTEM SOFTWARE

DAS Assemblers

Three versions of the Varian 73 DAS Assembler are available. DAS 4A is designed for a minimum system consisting of a computer with 4K memory and a teletype. DAS SA provides expanded capabilities for systems with at least 8K of memory, and utilizes additional peripheral devices, such as a rotating memory, magnetic tape transport, card equipment, paper tape system, or line printer.

The third and most comprehensive assembler is DAS MR, an integral part of the VORTEX and MOS operating systems. DAS MR is a macro assembler which produces relocatable object modules that may be loaded into any vector of the computer memory.

FORTRAN IV

Varian FORTRAN IV is an integrated software package that consists of a single-pass compiler for interpreting FORTRAN statements, converting them to machine-language instructions, a relocating loader for assembling object modules, and a run-time package that includes I/O drivers and a full set of arithmetic and data-conversion subroutines.

The package is available either as a stand-alone version requiring only 8K of memory, or as an integral part of the VORTEX and MOS operating systems.

BASIC

BASIC is an advanced version of the self-teaching system developed at Dartmouth College. It is applicable to a variety of business and scientific applications.

The programming language is simple and easy to use. Source statements are typed directly on a system console; if any errors are entered, the computer immediately responds and a correction can be made.

Extended BASIC

Extended BASIC expands the BASIC language to make it a more powerful tool for researchers. Special statements have been developed to facilitate the interaction between the computer and an external data-acquisition or process-control system. Other statements are designed to establish and control data files stored on a rotating memory device, and to facilitate changing of program overlay segments. Extended BASIC has been developed to operate with the ADAPTS hardware/software system.

RPG IV

Varian RPG IV (Report Program Generator) is a business-oriented language for preparing statistical data and tabular reports such as inventory records, sales analyses, and personnel summaries.

The Varian RPG IV compiler is an advanced version of RPG systems now widely used throughout industry for commercial applications. It is available either as a free-standing software package, or under control of the MOS batch operating system.

BEST

BEST (Basic Executive Scheduler and Timekeeper) is a real-time monitor that automatically schedules core-resident programs according to the time of day, at fixed time intervals, or at the earliest opportunity.

BEST can operate with any Varian 73 computer equipped with 4K of memory, making it a valuable addition to dedicated real-time computer systems.

Utility Programs

Varian 73 utility programs are standard software elements supplied (along with an Assembler) with every Varian computer.

BLD II is used to load object programs from a paper tape or TTY reader.

AID II is an on-line debugging program for correcting programming errors.

EDIT is used to add, delete, and correct any portion of a symbolic program.

MAINTAIN II checks that all hardware elements in the system are operating correctly.

MATH LIBRARY is a comprehensive set of mathematical function subroutines.

THE ALL-NEW VARIAN 73 . . . PACKAGED FOR RELIABILITY AND EASE OF EXPANSION

The Varian 73 incorporates a number of innovative packaging concepts, all aimed at increasing reliability and performance, as well as simplifying the task of system expansion or change.

For the first time, a truly universal mainframe backplane has been provided. All computer circuitry is mounted on large single-board modules. 15.6 inches by 19 inches, inserted through the front of the computer. The modules plug into a multilayer printed-circuit backplane which contains the dual memory buses and control signals. Any module can be placed in any slot position.

Connected to the front of the modules are flexible cables with controlled impedance for the I/O interconnections (Programmed I/O, DMA, High-Speed DMA, and PMA).

A valuable side benefit of this packaging technique is that no extender boards or other devices that might alter the computer performance are required for servicing the individual modules. The module is simply moved to the uppermost slot and with the computer chassis drawn out on slides, serviced from the top.

The combination of large board packaging and extensive use of MSI and LSI circuits has reduced both the component count and the path lengths between components. Wilh a minimum number of interconnections and board-to-board cabling, the Varian 73 represents an optimum design for reliable service.

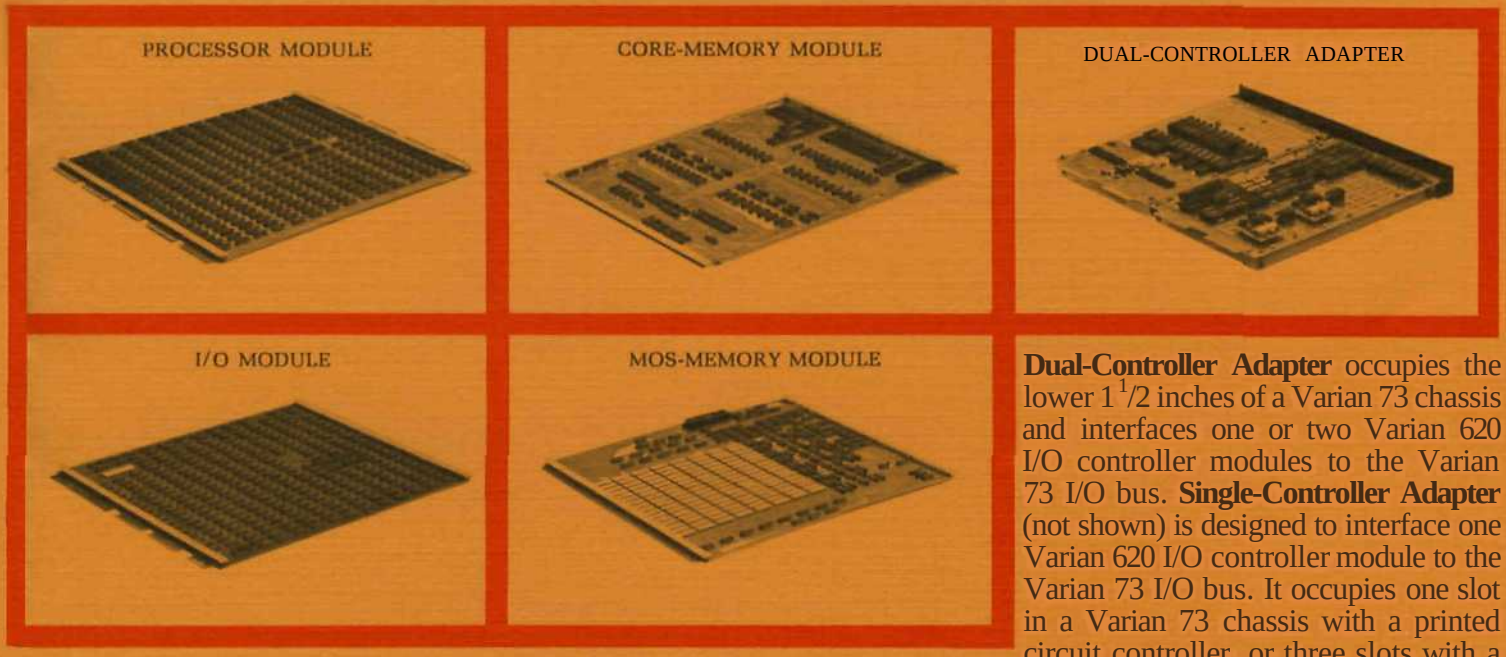
Two Mainframe Chassis — The systems designer has the choice of two Varian 73 mainframe chassis. The 7-inch chassis provides 7 slot positions plus space for two I/O controllers. The 14-inch chassis increases the slot positions to 17. A 32K MOS-memory system can be contained in the smaller chassis; a 120K system in the larger Additional memory can be housed in a second 7-inch or 14-inch chassis. If space is required for additional I/O controllers, a $10^{1}/_{2}$-inch I/O Expansion Chassis is used.

Two Mainframe Consoles — Two types of mainframe consoles are available. The Programmer's Console has all the controls and indicators needed to load and debug programs. The Operator's Console has only those controls needed to start and stop the computer. A key switch provides security for the program being run.

Power Supply — A separate $5^{1}/_{4}$-inch power supply can drive a full 32K system, core or MOS. A Power Failure/ Restart mainframe option provide protection against momentary loss of reduction of ac power. A Data Save option can be added to provide stand-by battery power for MOS memory modules.

Processor Module carries all central-processor circuits, including the 16 general-purpose registers, arithmetic and logical control unit, microprogram **ROM**, memory interface, and the data portion of the I/O interface.

Core-Memory Module carries 4K or 8K of dual-port memory, including all drive and control circuits. The first board occupies one slot in the mainframe or expansion chassis; succeeding boards occupy two slots.



I/O Module carries the control portion of the I/O interface, plus the Real Time clock, Power Failure/Restart, Teletype controller and such options as Memory Protect, Memory Parity, and Priority Memory Access.

MOS-Memory Module is available with IK, 2K, 4K, or 8K words. It occupies one slot in the mainframe or expansion chassis.

Dual-Controller Adapter occupies the lower $1\frac{1}{2}$ inches of a Varian 73 chassis and interfaces one or two Varian 620 I/O controller modules to the Varian 73 I/O bus. **Single-Controller Adapter** (not shown) is designed to interface one Varian 620 I/O controller module to the Varian 73 I/O bus. It occupies one slot in a Varian 73 chassis with a printed circuit controller, or three slots with a wire-wrapped controller. Additional I/O controllers can be individually housed in a separate $10\frac{1}{2}$-inch Expansion Chassis.

VARIAN 73 SPECIFICATIONS

Type	General purpose microprogrammed digital computer.
Memory, Semiconductor	Dual part semiconductor memory with 16-bit word length. Available in 1,021, 2,048. 4,096, and 8,192 word modules, with optional byte parity.
Memory, Core	Dualport magnetic core memory with 18-blt word length. Available in 4,096 and 8,192 word modules with optional byte parity.
Memory Size	Expandable to 32,768 words in any combination of semiconductor and core modules. Expandable to 65,536 words with Writable Control Store option. Expandable to 262,144 words with Future Memory Map option.
Word Length	Sixteen bits.
Registers	Sixteen general-purpose registers.
Arithmetic	Binary, two's complement.
Cycle Time	Semiconductor memory: 330 nanoseconds- Core memory: 660 nanoseconds.
Instruction Execution Time (Semiconductor Memory)	Register-register: 330 nanoseconds. Memory-register: 660 nanoseconds.
I/O Transfer Rate	DMA: 330,000 words per sec High-speed DMA: 1 million words per sec [SC memory] PMA: 3.03 million words per sec (SC memory)
Instructions:	159 standard, may be extended with Writable Control Store option.
Instruction Types	Single-word, addressing Single-word, nonaddressing Double-word, addressing Double-word, nonaddressing
Addressing Modes	Direct to 2,048 words Relative to P, X or B register to 512 words Pre Indexing with X or B Register Multilevel Indirect to 32,768 words Immediate Post Indexing with X or B Register Extended Mode to 32,768 words Microprogram addressing to 65,536 words with Writable Control Store option, to 262,144 words with Memory Map option
Logic Levels	Positive Logic: (Internal) True — TTL high level False - TTL low level Negative Logic: (I/O Bus) True — TTL low level False = +2.8V minimum, +3.8V maximum
Standard Features	HardwareMulliply/Divide Power Failure/Restart Real Time Clock Hardware Priority Interrupt
Computer Options	Writable Control Store Memory Map Memory Protect Buffered Interlace Controller (BIC) Automatic Bootstrap Loader (ABL) Buffered I/O Controller [BIOC] High-Speed Priority Memory Access (PMA)
Software	DAS Symbolic Assemblers FORTRAN IV: BASIC VORTEX MOS Master Operating System RPG IV:PERT BEST Math Library BLD II AID II EDIT MAINTAIN II
Dimensions	Mainframe and expansion chassis are 7 and 14 inches high. 19 inches wide, and 20.5 inches deep. I/O expansion chassis Is $10^{1}/_{2}$ inches high, 19 inches wide, and 16 inches deep
Input Voltage	105 to 125V ac or 210 to 250V ac, at 50 or 60 Hz.
Temperature Operating Storage	 0 to 50 degrees C — 20 to 70 degrees C
Humidity Operating Storage	 To 90 percent without condensation To 95 percent without condensation

All specifications subject to change without notice.

VARIAN 73
ASSEMBLER
INSTRUCTIONS

		Execution Times In Nanoseconds SC Memory	Core Memory
Load & Store Instructions			
LDA	Load A Register	660	1320
LDAI	Load A Register Immediate	660	1320
LDAE	Load A Register Extended	990	1980
LDB	Load B Register	660	1320
LDBI	Load B Register Immediate	660	1320
LDBE	Load B Register Extended	990	1980
LDX	Load X Register	660	1320
LDXI	Load X Register Immediate	660	1320
LDXE	Load X Register Extended	990	1980
STA	Store A Register	660	1320
STAI	Store A Register Immediate	660	1320
STAE	Store A Register Extended	990	1980
STB	Store B Register	660	1320
STBI	Store B Register Immediate	660	1320
STBE	Store B Register Extended	990	1980
STX	Store X Register	660	1320
STXI	Store X Register Immediate	660	1320
STXE	Store X Register Extended	990	1980
TSA	Transfer Switches to A Register	3300—3795	3341—3836
Arithmetic Instructions			
INR	Increment Memory and Replace	990	1980
INRI	Increment and Replace Immediate	990	1980
INRE	Increment Memory and Replace Extended	1320	2640
ADD	Add Memory to A Register	660	1320
ADDI	Add Memory to A Register Immediate	660	1320
ADDE	Add Memory to A Register Extended	990	1980
SUB	Subtract Memory from A Register	660	1320
SUBI	Subtract Memory from A Register Immediate	660	1320
SUBE	Subtract Memory from A Register Extended	990	1980
MUL	Multiply	4455—4950	4826—5321
MULI	Multiply Immediate	4290—4785	4661—5156
MULE	Multiply Extended	4785—5280	5486—5981
DIV	Divide	4785—5610	5156—5981
DIVI	Divide Immediate	4620—5445	4991—5816
DIVE	Divide Extended	5115—5940	5816—6641
Logic Instructions			
ORA	Inclusive-OR Memory and A Register	660	1320
ORAI	Inclusive-OR to A Register Immediate	660	1320
ORAE	Inclusive-OR Memory and A Register Extended	990	1980
ERA	Exclusive-OR Memory and A Register	660	1320
ERAI	Exclusive-OR to A Register Immediate	660	1320
ERAE	Exclusive-OR Memory and A Register Extended	990	1980
ANA	AND Memory and A Register	660	1320
ANAI	AND to A Register Immediate	660	1320
ANAE	AND Memory and A Register Extended	990	1980
Jump Instructions*			
JMP	Jump Unconditionally	701	1320
JOF	Jump if Overflow Indicator Set	701, 825	1320
JAP	Jump if A Register Positive	701, 825	1320
JAN	Jump if A Register Negative	701, 825	1320
JAZ	Jump if A Register Zero	701, 825	1320
JBZ	Jump if B Register Zero	701, 825	1320
JXZ	Jump if X Register Zero	701, 825	1320
JSS1	Jump if Sense Switch 1 Set	701, 825	1320
JSS2	Jump if Sense Switch 2 Set	701, 825	1320
JSS3	Jump if Sense Switch 3 Set	701, 825	1320
JIF	Jump if Combined Conditions Are Met	701, 825	1320
JANZ	Jump if A Register Not Zero	701, 825	1320
JBNZ	Jump if B Register Not Zero	701, 825	1320
JXNZ	Jump if X Register Not Zero	701, 825	1320
JS1N	Jump if Sense Switch 1 Not Set	701, 825	1320
JS2N	Jump if Sense Switch 2 Not Set	701, 825	1320
JS3N	Jump if Sense Switch 3 Not Set	701, 825	1320
IJMP	Indexed Jump	701, 825	1320
JSR	Jump Unconditionally and Set Return in Index Register	701	1320
JOFN	Jump if Overflow Indicator Not Set	825	1320
BT	Bit Test	1155—1320	1526—1691
SRE	Skip if Register Equal to Memory	1395—1650	2021—2186
Jump-And-Mark Instructions*			
JMPM	Jump and Mark Unconditionally	1196	1980
JOFM	Jump and Mark if Overflow Set	1196, 825	1980, 1320
JANM	Jump and Mark if A Register Negative	1196, 825	1980, 1320
JAPM	Jump and Mark if A Register Positive	1196, 825	1980, 1320
JAZM	Jump and Mark if A Register Zero	1196, 825	1980, 1320
JBZM	Jump and Mark if B Register Zero	1196, 825	1980, 1320
JXZM	Jump and Mark if X Register Zero	1196, 825	1980, 1320
JS1M	Jump and Mark if Sense Switch 1 Set	1196, 825	1980, 1320
JS2M	Jump and Mark if Sense Switch 2 Set	1196, 825	1980, 1320
JS3M	Jump and Mark if Sense Switch 3 Set	1196, 825	1980, 1320
JIFM	Jump and Mark if Combined Conditions Are Met	1196, 825	1980, 1320
JOFNM	Jump and Mark if Overflow Not Set	1196, 825	1980, 1320
JANZM	Jump and Mark if A Register Not Zero	1196, 825	1980, 1320
JBNZM	Jump and Mark if B Register Not Zero	1196, 825	1980, 1320
JXNZM	Jump and Mark if X Register Not Zero	1196, 825	1980, 1320
JS1NM	Jump and Mark if Sense Switch 1 Not Set	1196, 825	1980, 1320
JS2NM	Jump and Mark if Sense Switch 2 Not Set	1196, 825	1980, 1320
JS3NM	Jump and Mark if Sense Switch 3 Not Set	1196, 825	1980, 1320
Execution Instructions*			
XEC	Execute Unconditionally	701	1320
XOF	Execute if Overflow Set	701, 495	1320
XAP	Execute if A Register Positive	701, 495	1320
XAN	Execute if A Register Negative	701, 495	1320
XAZ	Execute if A Register Zero	701, 495	1320
XBZ	Execute if B Register Zero	701, 495	1320
XXZ	Execute if X Register Zero	701, 495	1320
XS1	Execute if Sense Switch 1 Set	701, 495	1320
XS2	Execute if Sense Switch 2 Set	701, 495	1320
XS3	Execute if Sense Switch 3 Set	701, 495	1320
XIF	Execute if Combined Conditions Are Met	701, 495	1320
XOFN	Execute if Overflow Not Set	701, 495	1320
XANZ	Execute if A Register Not Zero	701, 495	1320
XBNZ	Execute if B Register Not Zero	701, 495	1320
XXNZ	Executive if X Register Not Zero	701, 495	1320
XS1N	Execute if Sense Switch 1 Not Set	701, 495	1320
XS2N	Execute if Sense Switch 2 Not Set	701, 495	1320
XS3N	Execute if Sense Switch 3 Not Set	701, 495	1320
Control Instructions			
HLT	Halt	330	660
NOP	No Operation	330	660
SOF	Set Overflow Indicator	330	660
ROF	Reset Overflow Indicator	330	660
Shift Instructions**			
LSRA	Logical Shift Right A Register	495+	536+
LSRB	Logical Shift Right B Register	495+	536+
LRLA	Logical Rotate Left A Register	495+	536+
LRLB	Logical Rotate Left B Register	495+	536+
LLSR	Long Logical Shift Right	990+	1031+
LLRL	Long Logical Rotate Left	990+	1031+
ASRA	Arithmetic Shift Right A Register	495+	536+
ASLA	Arithmetic Shift Left A Register	495+	536+
LASR	Long Arithmetic Shift Right	825+	866+
LASL	Long Arithmetic Shift Left	825+	866+
ASRB	Arithmetic Shift Right B Register	495+	536+
ASLB	Arithmetic Shift Left B Register	495+	536+
Register-Change Instructions			
IAR	Increment A Register	330	660
IBR	Increment B Register	330	660
IXR	Increment X Register	330	660
DAR	Decrement A Register	330	660
DBR	Decrement B Register	330	660
DXR	Decrement X Register	330	660
CPA	Complement A Register	330	660
CPB	Complement B Register	330	660
CPX	Complement X Register	330	660
TAB	Transfer A Register to B Register	330	660
TAX	Transfer A Register to X Register	330	660
TBA	Transfer B Register to A Register	330	660
TBX	Transfer B Register to X Register	330	660
TXA	Transfer X Register to A Register	330	660
TXB	Transfer X Register to B Register	330	660
TZA	Transfer Zero to A Register	330	660
TZB	Transfer Zero to B Register	330	660
TZX	Transfer Zero to X Register	330	660
AOFA	Add Overflow to A Register	330	660
AOFB	Add Overflow to B Register	330	660
AOFX	Add Overflow to X Register	330	660
SOFA	Subtract Overflow from A Register	330	660
SOFB	Subtract Overflow from B Register	330	660
SOFX	Subtract Overflow from X Register	330	660
MERGE	Merge Source to Destination	330—825	660—1320
INCR	Increment Source to Destination	330—825	660—1320
DECR	Decrement Source to Destination	330—825	660—1320
COMPL	Complement Source to Destination	330—825	660—1320
ZERO	Zero Register	330—825	660—1320
I/O Instructions			
SEN	Program Sense	1980—2640	2351—3011
EXC	External Control	1980—2475	2021—2516
CIA	Clear and Input to A Register	1980—2475	2021—2516
CIB	Clear and Input to B Register	1980—2475	2021—2516
CIAB	Clear and Input to A and B Registers	1980—2475	2021—2516
INA	Input to A Register	1980—2475	2021—2516
INB	Input to B Register	1980—2475	2021—2516
INAB	Input to A and B Register	2145—2640	2185—2681
OAR	Output from A Register	2310—2805	2351—2846
OBR	Output from B Register	2310—2805	2351—2846
OAB	Output from A and B Registers	2310—2805	2351—2846
IME	Input to Memory	2640—3135	3341—3836
OME	Output from Memory	3135—3630	3671—4166

* First time is for condition true (for each indirect level add 371 ns for SC memory, 660 ns for core memory). Second time is for condition not true.

** For n shifts, add 165n nanoseconds.

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