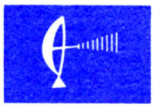
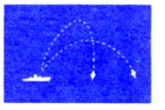
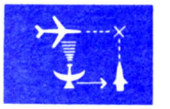
64-1411


Radar Data Processing


Trajectory Computation


Navigation

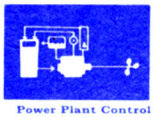

Fire Control


System Checkout


Inventory Control


Preventive Maintenance

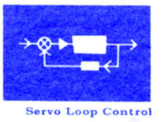

Range Safety

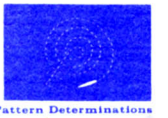

Power Plant Control


Personnel Records


System Simulation


Data Reduction and Processing


Servo Loop Control


Pattern Determinations

AN/UYK-1

A Multiple Purpose Digital Computer

RAMO-WOOLDRIDGE a division of Thompson Ramo Wooldridge Inc.

AN/UYK-1

A "STORED LOGIC" MULTIPLE PURPOSE COMPUTER

A
STORED
LOGIC
MULTIPLE
PURPOSE
DIGITAL
COMPUTER

APRIL 21, 1961

RAMO-WOOLDRIDGE a division of Thompson Ramo Wooldridge Inc.

8433 Fallbrook Avenue, Canoga Park, Calif.

AN/UYK-1, A Stored Logic Multiple-Purpose Digital Computer

CONTENTS

1. INTRODUCTION

The AN/UYK- 1 Shipboard digital computer, developed by Ramo-Wooldridge for the Bureau of Ships under contract NObsr 81349, is small, inexpensive, and highly adaptable to the solution of many of the Navy's computer problems. This computer is based on a new digital technique called "Stored Logic" which achieves user convenience, adaptability, and low cost by allowing the instantaneous logical organization of the computer to be specified as part of the program.

The AN/UYK-1 is compatible with NTDS and is designed to meet NAVY environmental requirements for shipboard or land-based use.

1.1 GENERAL CHARACTERISTICS OF THE AN/UYK-1

The AN/UYK-1 is a stored logic digital computer that is:

Rugged. It can operate in shipboard or land-based environments.

Inexpensive. It is economically justified even for relatively small tasks.

Easy to Use. It can be used by people who are not computer experts to solve their problems.

Small. It can fit aboard even small naval vessels.

Compatible with NTDS. It can use NTDS peripheral equipment and can supplement the AN/USQ-20 computer.

Capable. It can do many jobs because of its special data processing capability and 8192 word core memory.

Multipurpose. It is readily adapted to meet many of the Navy's computer needs.

The AN/UYK-1 is a multiple purpose, rather than a special or general purpose computer because the user can choose a set of simple, easily understood instructions tailored to fit his specific problem. For example, an instruction which can be made available is CTRP -- Coordinate Transformation from Rectangular to Polar (i.e., x, y to r, θ). The user need not be a highly skilled programmer; he merely enters the coded designation of the instruction, where to find x and y, and where to place r and θ, in the memory. The stored logic program causes the computer to perform the complicated operations of the transformation equations automatically, leaving the user free to concentrate on the job to be done and the source and destination of the data being processed.

1.2 STORED LOGIC - ADAPTABILITY AT LOW COST

The AN/UYK-1 is economical, reliable and small, and has relatively few components because it is organized as a parallel 15-bit word element machine. Although 15-bit arithmetic is suitable for some jobs, many problems and full compatibility with NTDS computers require longer words. This compatibility is inherent in the design of the AN/UYK-1 Computer. It is achieved by efficiently manipulating 15-bit word elements to operate as a 30-bit word fixed point or 45-bit floating point computer or as a character data processor.

Data manipulation is controlled by words stored in memory. These controlling word elements are called logands and a sequence of logands making up the complex instructions is called a logram. The user need never know the details of the lograms since the computer is designed to sequence from logram to logram automatically with no burden of book-keeping on the user.

Logands are simple operations such as "load a register" or "shift a register" and the logic for mechanizing them is built into the hardware. The control logic, therefore, is unusually simple and the computer relatively easy to test and maintain.

The computer can operate in a number of modes that trade ease of use for operating speed. For example, the user can write a program using logands directly for very high speed operation, or he can use lograms to generate powerful multiple address instructions providing for indirect and indexed addressing. In such instructions, any word in memory can be used for an index register or to hold an indirect address.

The term "stored logic" has been used to describe this computer because the sequences required to perform instructions are stored as logands in the core memory. A typical set of lograms will take up less than 10 percent of the memory.

1.3 DATA PROCESSING FEATURES

The AN/UYK-1 speeds the processing of data by reacting quickly and automatically to external control signals and by providing special logands to manipulate blocks of information. For example, the AN/UYK-1 can compare a number with a 1000-word random table, five times faster than the most commonly used large-scale computer.

1.3. 1 External Control

External control signals to which the computer is responsive are "Interrupt" and "Data Input-Output". These signals cause the computer to interrupt and execute a subroutine specified by the interrupting device. A data input output routine may transfer any number of words between the external device and memory with the length of transfer

specified by the external device. After completing the interrupt subroutine or the data transfer, the computer resumes the interrupted computation without loss of intermediate results.

1.3.2 Special Logands

The special logands to manipulate multi-word blocks include:

Block Transfer. Transfers a block of data from one location to another within memory.

Block Input-Output. Transfers a block of data between memory and an external device. (The length of the transfer is specified by the computer.)

Table Look-Up. Conditionally compares a computer word sequentially with the words of a block. The program branches when the condition is met or the end of the sequence is reached. This logand is very powerful for sorting and merging operations.

Match. Conditionally compares two sequences of computer words. The program branches when the condition is not met. This logand is especially useful for comparing a set of results against upper or lower limits or for searching for a multi-word key.

The available comparison criteria for Table look-up and Match include equality, inequality, greater than and less than.

These special logands, coupled with the flexibility of logand control, make the AN/UYK-1 faster and easier to use for complete data processing tasks than more expensive machines.

1.4 INPUT-OUTPUT

The AN/UYK- 1 can communicate directly with NTDS peripheral equipment by parallel 30-bit words. A 15-bit register is also provided parallel transfers to other devices such as paper tape and teletype units. External devices can establish communications by computer interrupts and can control the data transfer rate.

1.5 PACKAGING

The AN/UYK-1 will operate in adverse environmental conditions with minimum maintenance. The design has included provisions for the structural rigidity to meet Navy shock and vibration specifications. Insert cards are held rigidly by precision side guides and rugged hold-down bars. Special attention has been given to the practical aspects of the machine's use: access to all elements is from the front; test points

for all active circuits are available; the control panel is very simple; a maintenance panel is built in; there are no sharp corners that could injure personnel; cable access is convenient. In short, the computer has been designed to be easy to use and maintain.

2. SIGNIFICANT FEATURES OF LOGICAL DESIGN APPROACH

It is convenient to review the definition of several new terms before attempting a more detailed description of the AN/UYK-1.

a. LOGAND. Contraction of "Logical command", an elementary operation which causes a combination of transfers, decisions, and elementary control sequences in a computer terminating in "read the next logand. " It is distinguished from an ordinary computer instruction in that it requires significantly less complex wired-in logic.

b. LOGRAM. A sequence of logands ("logical program") which when executed result in a computer operation similar to but usually more powerful than that done by a conventional computer instruction.

c. STORED LOGIC. The sequence of logands comprising a logram will be stored in the core memory in the AN/UYK-1. Since the whole sequence is used to accomplish an operation ordinarily done with wired-in logic, the AN/UYK-1 is called a "stored logic" machine.

Conventional computer instructions are complex operations resulting from sequences of simple operations. The sequence is unique for each instruction and is called out by the instruction code. Sequencing is automatic to provide high speed operation. Economy dictates that the number of such automatic sequences (instructions) be limited and certain restrictions be put on the user (e. g. , that it is a single address machine) which force constraints on the programmer.

Many of these constraints can be removed if each of the detailed steps in the instruction sequence is separately programmed and new sequences to meet new requirements provided by programming. Detailed programming of each instruction sequence places unacceptable requirements on the programmer which make the technique unsuitable. However, the important fact which makes such a machine possible also makes the stored logic machine possible -- any conceivable computer instruction can be synthesized by a sequence chosen from a suitable small set of minimal control functions.

The flexibility of logram control makes several desirable programming features feasible. For example, the number of addresses in the instruction can be made to depend on the instruction. Arithmetic instructions can have three addresses, while transfer instructions have two addresses and shift instructions have a single address. Lograms can be written to generate any desired instruction with any number of addresses.

An interesting consequence of the flexibility of logram control is that new kinds of instructions, which are not normally considered economic but are highly convenient, can be provided at no additional hardware

cost. Examples illustrating the possibilities are the design of instructions using index registers in more powerful ways to assist the programmer in automatically processing library sub-routines and indexing on the sum of two index registers to facilitate matrix manipulation.

Some insight into the operation of the stored logic machine can be gained by considering the kinds of operations which must be performed in executing a typical instruction from a program. The programmer might write:

> Add X/ to Y/ and store sum in Z/ where X/ = the contents of storage location X, etc.

The computer will interpret "Add" as the starting address of the add logram and X, Y, and Z as operand locations. Control will transfer (under control of the last logands in the previous logram) to the add logram which will manipulate X/, Y/, and Z/ as required, retain the program location, and set up entry into the logram specified by the next instruction.

It is anticipated that a typical set of lograms will occupy about 10 percent of the core memory.

Programmers will ordinarily work with a list of lograms analogous to an instruction list and with a library of subroutines made up of lograms. Lograms will be assembled by the logical designer or a skilled programmer. Since a new logram or set of lograms does not involve hardware changes, the AN/UYK-1 "instruction list" can be changed at any time just by loading a new set of lograms into the memory from the associated input equipment.

The 15-bit word element length of the AN/UYK-1 was chosen for economy in consideration of the required computer precision of 30 bits. In essence the machine is always operated double precision when 30 bits are required, however, the flexibility of stored logic control makes the AN/UYK-1 very fast on double precision operations and makes it unnecessary for the user to be aware of the internal manipulations by 15-bit word elements.

The entire word element can be used to specify a memory location hence the proposed 8192 word element memory {4096 30-bit words) can be expanded almost arbitrarily without change in the logical design of the machine.

The 15-bit elementary word length also has a number of other advantages. The AN/UYK-1 may be logrammed for 15-bit arithmetic, which is adequate for calculations involving physical measurements, with an increase in calculating speed. It may be logrammed for 30- or 45-bit arithmetic where increased precision is required. Or it may do floating-point calculations with a 15- or 30-bit mantissa and 15 bits of exponent.

The flexibility of the stored-logic approach can be illustrated by consideration of a variety of possible applications for the AN/UYK- 1:

a. One-time solution of a complex analytical problem. In this application programming cost tends to be much more expensive than computer time. To hold programming time to a minimum, the AN/UYK-1 would be logrammed for floating-point arithmetic operations of 30-bit accuracy, thereby saving the programmer the problem of scaling his variables to keep them in range of computer operations. The instructions lists would be kept small so that the programmer's learning task is easy and logram storage is small. In comparing the AN/UYK-1 to a fixed-point conventional computer which may be subroutined for floating-point operations, the significant advantage of the AN/UYK-1 is that the floating-point lograms will decrease the AN/UYK-1 speed by a smaller percentage than a more conventional machine.

b. Compilation of a table showing the value of some function for a large number of discrete values of the argument. If the function to be computed is not too complex, programming is not a very big job and a fixed-point set of lograms would be used to reduce computing time. The instruction list would still be kept small so that the programmer is not burdened with learning (perhaps not too thoroughly) many different instructions for accomplishing not-very-difficult operations.

c. On-line application in which the computer stands ready to compute a set program as input data is made available to it. Fixed-point operation in the interest of speed of calculation is best here. If the on-line program is likely to be kept in the machine for a long period with only minor modifications from time to time, it might be worthwhile to design the logram list to best suit the program. If the program will be changed every month or so, a versatile "universal" set of lograms would be provided to the programmer. If the input variables are derived from measurement of physical parameters, 15-bit accuracy will very likely be sufficient and computing speed would be thereby increased.

d. A high-speed filing system. In this case the computer would be logrammed for sorting, collating, search, and data transfer operations. Use of the special logands for data processing would allow very efficient solution of these problems.

e. Combined on-line and problem-solving operations. It might be desired that the computer be instantaneously available for an on-line computation, but the application involves a lot of idle time, which might be used for solution of a complex analytical problem. The instruction list would include both fixed-point operations for the on-line program and floating-point operations of perhaps greater accuracy for the analytical program. The instruction list and on-line program would remain in the machine at all times and varying analytical programs could be loaded in as required. Call for an on-line computation would interrupt the analytical program, which would be resumed as soon as the on-line computation was completed. For this application, it might well be desirable to extend the memory to 16, 384 or 3 2, 768 15-bit words.

3. USER'S VIEW OF THE AN/UYK- 1

3.1 OPERATION FEATURES

Large-scale digital computers are run by full time, specially trained operators. Ideally, the AN/UYK- 1, on the other hand, would best fulfill its intended role if it required no more attention than, say, a motor-generator set. Practically, the operator will have to know how to load punched paper and magnetic tape transports (if used) and understand a few simple controls on the computer. The design of the AN/UYK-1 control panel has been based on these principles:

a. Minimum number of controls

b. Familiar elements (simple toggle and push-button switches and indicating lights)

c. Familiar and descriptive labels and legends

d. Logical arrangement

The controls on the operator's panel are:

(1) A power switch (circuit breaker) and indicating light.

(2) 15 toggle switches arranged in a row.

(3) 15 neon lights arranged in a row to correspond with the 15 toggle switches.

(4) A name card holder so that a card identifying specific functions for the switches and lights can be inserted.

(5) A push button.

The 15 toggle switches permit manual inputs into the computer. When the push button is operated, the computer is interrupted and the number set into the toggle switches is read into the computer. The function of the toggle switch register is therefore specified by program control. All normal use of the machine including entry of new programs is controlled in this manner.

If for any reason the loading program must be entered into the machine the maintenance loading switch on the maintenance panel must be set. The push button then serves to set all required flip-flops to start reading in a bootstrap loading program which in turn loads the loading routine. The computer can be started by this simple procedure even if it has a cleared memory.

The neon lights are a remote indication of the states of the flip-flops in the E register and serve as a convenient means of communication between the operator and the program.

3.2 PROGRAMMING CHARACTERISTICS

By its nature, the AN/UYK-1 has a two-level programming structure. First, lograms are written using the logands which are the computer's basic language. Once a sufficient set of lograms is written, all programs can be written using only lograms. This process is analogous to present programming where compilers convert symbolic programming to machine language.

The elemental word length of the AN/UYK-1 is 15 bits. The basic memory is 8, 192 of these words. The memory can be expanded almost arbitrarily without changing the structure of the machine. Thirty-bit numbers occupy two AN/UYK-1 words. Lograms may be written for 15, 30, or 45 bit numbers as required by the application.

Suppose a two-address ADD REPLACE operation is required, with the second address indexed by the contents of an arbitrary memory cell i. Symbolically, this can be expressed:

$$g/ + (h + i/) / \longrightarrow h + i/$$

where g and h are the operand addresses and g/ means "the contents of g. " In programming the AN/UYK-1, the programmer would write the following:

Address	Contents of cell
a	Logram address
$a + 1$	g
$a + 2$	i
$a + 3$	h
$a + 4$	Next logram

The "logram address" is the address of the first logand of the ADD REPLACE operation. The logram will interpret the following addresses to obtain the operands and index register contents. In this example the index register may be any cell in the core memory, hence there is no limit on the number of index registers which may be used.

A typical problem will demonstrate the flexibility and useability of the AN/UYK-1's structure. Suppose that the solution to the function G = X^2 Y + A cos X is required for 100 values of X and 10 values of Y and all numbers are scaled appropriately. In the following table, a plain-English description of the program is given in the first two columns, while the last two describe symbolically the program as written by the programmer. Symbols are used as follows:

α : Address of the first instruction of the program

$X_i/^{-1}$: Address of the ith value of X

$X_o/^{-1}$: Address of the initial value of X

$I_1/$: First Index

I_1: Address of first index

F: Arbitrary cell used for intermediate storage

F/: The number stored in F

Program Step	Description	Machine Address	Contents
1.	Read 100 words from paper tape, storing them in locations $X_i/^{-1}$	α α + 1 α + 2	READ PAPER TAPE (0) $X_o/^{-1}$ 100
2.	Read 10 words from paper tape, storing them in locations $Y_i/^{-1}$	α + 3 α + 4 α + 5	READ PAPER TAPE (0) $Y_o/^{-1}$ 10
3.	Set the contents of α + 5 into location I_2	α + 6 α + 7 α + 8	SET (0) α + 5 I_2
4.	Set the contents of α + 2 into location I_1	α + 9 α + 10 α + 11	SET (0) α + 2 I_1
5.	Compute cosine of X_i and hold in accumulator	α + 12 α + 13 etc.	COSINE (I_1) $X_o/^{-1}$ ACC.
6.	Compute A cos X_i and store in F		MULTIPLY (0) $A/^{-1}$ F
7.	Compute X_i^2 and hold in accumulator		SET (I_1) $X_o/^{-1}$ ACC. MULTIPLY (I_1) $X_o/^{-1}$ ACC.

Program Step	Description	Machine Address	Contents
8.	Compute $Y_j X_i^2$ and hold in accumulator		MULTIPLY (I_2) $Y_o/-1$ ACC.
9.	Add F/ to Accumulator to get G, store in F		ADD (0) F F
10.	Punch F/=G		PUNCH (0) F 1
11.	Punch X_i		PUNCH (I_1) $X_o/-1$ 1
12.	Punch Y_i		PUNCH (I_2) $Y_o/-1$ 1
13.	Decrement I_1/ and Test for 0. If ≠ 0, go back to STEP 5		INDEX (I_1) $\alpha + 12$
14.	Decrement I_2/ and test for 0. If ≠ 0, go to STEP 4		INDEX (I_2) $\alpha + 9$
15.	Next routine.		

Notice that in this example two-address instructions are used; one address is used for one of the operands, the other for the result. The index register is specified in the same word as that used to give the logram address. A zero in parenthesis after the name of the logram means no indexing. Also, notice that the programmer is not concerned about numbers requiring two memory cells. The indexing logram automatically makes the required address modification.

From the example it can be seen that the logram structure enables the programmer to be sophisticated but keep programs simple. Only the lograms, which like subroutines are only written once, are complicated. It might be noted that floating point arithmetic could be used without a significant increase in program running time. Typical logram times are given in the Summary of Characteristics, Section 5.

3.3 MAINTENANCE ASPECTS

Solid-state digital computers are developing better and better reliability records; they are not and probably never will be completely free from

failures. When failures do occur, the problem is to find the specific point of failure; repairing it is usually trivial. Diagnostic routines can be of some help in localizing the trouble, but the final pinpointing still requires a human being with an understanding of the machine. The stored-logic approach used in the AN/UYK-1 promises to minimize the maintenance man's learning task in two ways:

a. It is a parallel machine and parallel arithmetic leads to many repetitions in the hardware structure.

b. Only elementary logical operations are implemented with hardware. Complexity is in the logand sequences.

Certain controls are provided exclusively for maintenance purposes in the AN/UYK-1; these are located behind an access door on the control panel. The maintenance man also uses the operator's controls. The following are on the maintenance control panel.

Running time meter

Voltmeter and selector switch

Pushbutton switches for:

1. Single clock
2. Single logand
3. Address search
4. Flag stop

Primary mode toggle switches:

1. Automatic-manual
2. Normal-maintenance loading

Power supply marginal check switches

Transfer pushbuttons

1. E ⟷ L
2. Switches → E
3. E ⟷ A
4. E ⟷ M
5. E ⟷ P
6. E ⟷ T

7. Clear core and write E

8. Clear E, read core and rewrite

Test Jacks on clock, power supply voltages, synchronization signals, etc.

These controls are sufficient to provide the maintenance man with the capability for complete manual control of all phases of machine operation and provide flexibility for quick diagnosis of failures.

Every insert card has test points accessible without removing the card. Power supply test points are provided on the maintenance man's control panel. All test points are immediately in front of the maintenance man when he opens the doors on the front of the cabinet.

Register and control indication are by neon lights mounted on the flip-flop cards. Flip-flop cards are assigned to slots in such a manner that the lights present a meaningful array.

Maintenance data is organized in three lists:

1. Logical equations with test points

2. Wiring by wire name

3. Wiring by connector

The first list is used in tracing a trouble through the logic and gives the location of a test point at which the level of any gate in the system can be monitored. Brief explanatory notes on this list describe the functions of the various logic terms.

The other two lists are printed from duplicate decks of punched cards sorted in two different ways. Each card gives the location of a wiring connection point and the name of the wire connecting to that point. The second list groups these cards by wire name so that all points to which a wire connects may be determined. The third list groups the cards by location so that the name of a wire can be determined.

In addition to these lists the maintenance man is provided with a chart showing the logical names and locations of all component circuits and schematic drawings of all cards.

Since all component circuits, with the exception of the power supplies, are mounted on insert cards, repair may be effected by replacing a bad card with a good one. Bad cards can be returned to a higher echelon depot or Ramo-Wooldridge for repair, if desired. Cards may also be repaired in the field. Card extenders permit the malfunction to be traced to a particular component while the circuit is in operation in the machine.

3.4 NTDS COMPATIBILITY

The AN/UYK-1 will be compatible with the Navy Tactical Data System. The computer will input or output 30-bit words in parallel in NTDS format at the proper signal levels. The appropriate synchronizing signals will also be furnished.

These features will enable the AN/UYK-1 to use all NTDS peripheral equipment and to supplement the AN/USQ-20 Computer where required.

4. FUNCTIONAL DESCRIPTION

4. 1 SYSTEM DESIGN

The equipment requirements for a "stored logic" computer are delineated by functional groups and illustrated by the block diagram of Figure 4-1. The principal functional groups together with a description of the usual functions are given below:

a. Initial core memory with storage for 8192 15-bit words, Matrix switch for selecting one of 8192 addresses. Fifteen sense amplifiers and fifteen inhibit drivers. Four timing generators.

b. Six fifteen-bit flip-flop registers for all internal data processing and handling. One set of fifteen full adders and one set of 15 half-adders (for optional counting transfers). Transfer logic for register transfers.

c. Control flip-flops for in-out controls and internal control and timing. Control logic and special circuits for input-output functions.

d. Power supply and clock generator.

The computer clock is at 333 kc per second; the memory read-write cycle requires six microseconds.

Brief tentative descriptions of the registers and associated transfer logic follow:

(1) L Register: Contains the logand being executed. A portion of the L Register can address a small part of the core memory. Accepts transfer from E and holds.

(2) E Register: Communicates with the core memory. Accepts transfers from cores, from the A, P, M, L, and T registers and holds.

(3) M Register: Addresses the core memory, and is also used for storage in arithmetic operations. Accepts transfers from E, A, or P and holds. The source of counting transfers to M, A, or P.

(4) P Register: Accepts transfers from M, E, and A registers, holds, shifts left and right.

(5) A Register: The active accumulator-also used for temporary storage. Accepts transfers from M, P, and E registers and full adders, clears, holds, shifts left and right, and inverts its own contents.

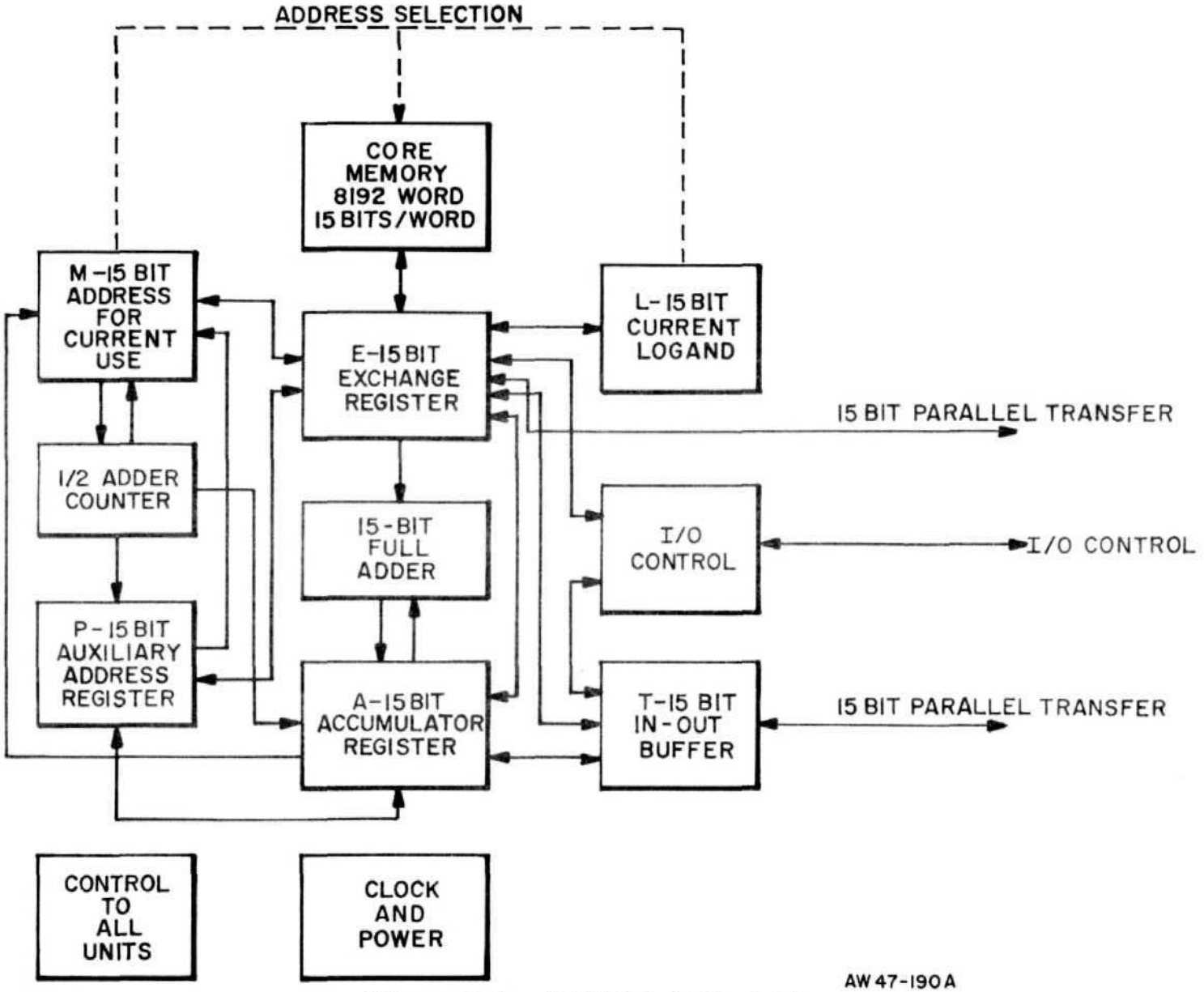


Figure 4-1. AN/UYK-1 Block Diagram

(6) T Register: Fifteen-bit input-output buffer register. Accepts transfers from external data lines, A or E registers, and holds. Most internal computer operations can proceed in a regular manner while the T register is communicating with slow-speed peripheral equipment.

In addition to the active registers enumerated above, 64 cells in the core memory may be addressed directly by the logand (without reference to the normal address register) and may be considered to be auxiliary registers. Some of these cells may be used as index registers and others as accumulators for numbers of 30 bits or more (the active accumulator holds only 15 bits). Still others may be used to hold partial products and intermediate remainders in multiplication and division, and to temporarily hold the address of the next instruction. These cells have an important use as index locations for interrupt and buffered input-output instructions.

The logands mechanized in the AN/UYK-1 are interpreted in three fields:

(1) The Address Option (AO) field - 3 bits

(2) The Primary Command (PC) field - 6 bits

(3) The Secondary-Address (SA) field - 6 bits

The first two clocks of every logand sequence are used to read from memory the contents of the cell specified by the M register, restore this word and transfer it to the L Register as the logand controlling the remainder of the cycle. The AO field of the logand specifies the general structure of the machine for the remainder of the logand cycle including the length of the cycle (4 or 6 clocks), the source of addresses for subsequent memory accesses and the automatic incrementing of calling, logand, and operand sequences.

The eight options of the AO field are:

1. DS (Direct addressing from L). With this option, the logand cycle is 4 clocks. The memory access for the operand during clocks 3 and 4 is addressed from the SA field of the logand (one of the least 64 cells in memory) and the contents of M are incremented thereby preparing the machine to read a logand from the cell following the cell containing the current logand.

2. DM (Direct addressing from M). With this option, if the current logand is stored in location Y, the operand address is Y+1 and the machine is prepared to read the next logand from Y+2. This option requires 4 clocks.

3. DP (Direct addressing from P). With this option, if the current logand is stored in location Y and an operand address Q is stored in the P register, the operand address will be Q and the machine will be prepared to take its next logand from Y+1 and will have Q+1 stored in its P register at the start of the next

cycle. This provides for automatic incrementing of two address strings. This option requires 4 clocks.

4. DA (Direct addressing from A). This option is like 3 above if P is replaced with A. This option is useful when the desired address is generated by an arithmetic operation.

5. IS (Indirect addressing from L). This option and all the indirect options require 6 clocks and define two memory accesses in addition to the logand access. With the IDL option, the second access is addressed by the SA field of the logand and the third access {for the operand) is addressed by the number obtained by the second access. At the end of the cycle the machine is prepared to read the next logand in sequence and has stored in its P register the contents of the cell addressed by the SA field plus 1. The logand and operand sequences have been automatically incremented,

6. IDM (Indirect addressing from M). With this option if Y is the address of the logand the second access will be from Y+l and the operand address will be from Y+l/ (read the contents of Y+l/). The machine will be prepared to take the next logand from Y+2 and will have the incremented operand address stored in its P register.

7. IDP {Indirect addressing from P). With this option, if Y is the address of the logand and Q is an address stored in the P register, the second access will be from Q and the operand address will be Q/. At the end of the logand sequence, the machine will be prepared to read the next logand from Y+l and Q+ 1 will be stored in the P register and the operand address plus one will be in the A register.

8. IDA (Indirect addressing from A). This option is like (4) above if Q is contained in A initially.

The PC field of the logand specifies the command to be performed during the logand cycle. The SA field is used as an address in the DS and IS address options, otherwise it may be used as a secondary command executed after the primary command. The basic logands are listed in Table 4. 1-1 together with the cycle time of execution and the type of implied memory cycle. A transfer into the A register specified by a command in the SA field has precedence if it conflicts with an automatic transfer specified in the AO field.

Table 4.1-1 Basic Logands

Command or group name	Transfers specified by command	Memory access implied	Time of execution			
			Direct cycle		Indirect cycle	
			PC	SA	PC	SA
LOAD		READ				
LA	E ⟶ A		3	4	5	6
LM	E ⟶ M		3	4	5	6
LP	E ⟶ P		3	4	5	6
LT	E ⟶ T		3	4	5	6
LE	E ⟶ E		3	-	5	-
STORE		WRITE				
SA	A ⟶ E		3	-	5	-
SP	P ⟶ E		3	-	5	-
ST	T ⟶ E		3	-	5	-
SE	E ⟶ E		3	-	5	-
REPLACE		READ				
RA	E ⟷ A		3	-	5	-
RM	E ⟷ M		3	-	5	-
RP	E ⟷ P		3	-	5	-
RT	E ⟷ T		3	-	5	-
STORE and HOLD		WRITE				
HA	E ⟷ A		3	-	5	-
HM	E ⟷ M		3	-	5	-
HP	E ⟷ P		3	-	5	-
HT	E ⟷ T		3	-	5	-
EXCHANGES		READ				
AP	A ⟷ P		3	4	5	6
AT	A ⟷ T		3	4	5	6
LOGICAL		READ				
XA	E.A' ⟶ A		3	4	5	6
MA	EvA ⟶ A		3	4	5	6
XE	E.A ⟶ E		3	-	5	-
DX	E.A' ⟶ A E.A ⟶ E		3	-	5	-
ME	EvA ⟶ E		3	-	5	-
ADD		READ				
AS	A+E ⟶ A C=1		4	4	6	6
AL	A+E ⟶ A C=1		4	4	6	6
AM	A+E ⟶ A C=C		4	4	6	6
AI	A+E ⟶ A C=C					

Table 4.1-1 Basic Logands (cont'd)

Command or group name	Transfers specified by command	Memory access implied	Time of execution			
			Direct cycle		Indirect cycle	
			PC	SA	PC	SA
COMPLEMENT						
CS	A' ⟶ A C=1		3	4	5	6
CC	A' ⟶ A C=0		3	4	5	6
CH	A' ⟶ A C=C		3	4	5	6
CLEAR						
ZE	Zeros ⟶ E		3		5	
SHIFTS						
SO	Logical, open ended		3a*	-	-	-
SC	Logical, closed		3a	-	-	-
SN	Numeric, open ended		3a	-	-	-
MP, MS	Multiply		3a	-	-	-
DV	Divide		3a			
FL	Float left		3a			
RC	Repeat Count M		3a	-	-	-
CONDITIONAL						
BR	Branch	READ	4	-	4	-
SK	Skip		4	-	4	-
PROCESSING						
TB	Table lookup	READ	-	-	-	-
MH	Match	READ	-	-	-	-
MV	Int Trans	READ	-	-	-	-
SR	Sort	READ	-	-	-	-
INPUT-OUTPUT						
CO, EF	1/0 control		3a	-	-	-
WO, WI	Word I/0	READ	3a		5a	
BO, BI	Block I/0	READ		-	-	-
IT	Initiate interrupt	WRITE/ READ	-	-	-	-
TM	Terminate interrupt	READ/ READ	-	-	-	-

*where a defines a holding state used for synchronization or counting.

A number of special logands which do not fit into the AO field control structure are also available. These logands rely on AO control of transfers only through the second clock time and then imply transfers which differ from the AO implied transfers. In many cases, control states are repeated so the logand controls for more than 4 or 6 clocks. Table 4. 1-2 lists these special logands, gives a brief description of the function of each, and the execution time.

4. 2 CIRCUITS

The circuits developed for the AN/UYK-1 computer use MIL Specification components to the greatest practical extent. Semiconductors are purchased to Ramo-Wooldridge specifications drawn to insure optimum circuit performance and reliability and to avoid the hazards of sole source procurement. Spare parts lists will, however, refer to commercial semiconductor part numbers for convenience in Government spare parts procurement.

All circuit cards have test connectors at the front of the card for monitoring input and output levels and significant internal points. Logic cards have test points on all gate centers.

Brief descriptions of the circuits follow:

a. Set-Reset Flip-Flop. This six-transistor clocked flip-flop is capable of operating at rates up to 700 kc per second. Input and output buffering stages isolate the basic flip-flop stage from the effects of variable line impedences. The output stages can drive resistance loads as low as 180 ohms. Output capabilities and input requirements are such that one flip-flop can drive about 20 other flip-flops. The set-reset flip-flop has two inputs ("Set" and "Reset") and two outputs (normal and complementary).

b. Delay Flip-Flop. This circuit differs from the set-reset flip-flop only in the input stage, which is arranged so that the flip-flop responds to the condition of a single input line for both setting and resetting. Both types of flip-flops are packaged two to a card.

c. Control Amplifier. This amplifier supplies current to activate a group of gates which act in convert. One is used for each register transfer. The control amplifier is not clocked and has a response time of less than 1. 0 microseconds. It is packaged three circuits to a card.

d. Sense Amplifier. This circuit detects the readout of data from the core plane representing one bit at all addresses in the memory core matrix. If the amplified signal exceeds the decision level at the strobe time, a pulse is transmitted to set a data register flip-flop.

e. Core Selection Switch. Address register flip-flops are decoded in this circuit "to" select one read-write drive line on each

Table 4.1-2 Special Logands

Command or Group Name	Brief Description of Operation	Execution Time (microsec.)
SHIFT	SA Determines direction, length, and registers	12 + 3n n = number of shifts or counts
SO	Logical (Shifts all bits of A), open ended	
SC	Logical, closed (most and least bits linked)	
SN	Numeric (A is shifted as a number), open ended	
MP, MS	Multiply	
DV	Divide	
FL	Float left	
RC	M + 1 M	
CONDITIONAL	SA Determines particular conditions	
BR	M + 1/ M Specified word element used as conditional next address	12 or 18
SK	M + 2 M Next address conditionally skipped	12 or 18
DATA PROCESSING	SA Determines condition for stopping	
TB	One word element compared to a sequence of known length	18 + 12n n = length of sequence
MH	Two sequences matched until the condition is satisfied	18 + 12n n = length of sequence
MV	A block of data of known length transferred from one location to another within memory	18 + 12n n = number of words in block
INPUT-OUTPUT		
CO, EF	SA transmitted to I/O control	12 (minimum time)
WO, WI	Single word element input/output	12 or 18
BO, BI	Block input/output (known length)	18 + 12n n = number of word elements
IT	Interrupt	18
TM	Terminate Interrupt	18

of two axes of the memory core matrix. Timing pulses from the read pulse generator and write pulse generator cause the switch to drive read and write currents through the selected lines in the matrix. The complete switch requires 20 cards of two kinds.

f. Inhibit Driver. Each memory core plane, corresponding to one bit at all addresses, has an inhibit winding used during the write cycle. If a zero is to be written, a current pulse from the inhibit driver for that bit prevents writing of a one in the selected core. Inputs to the inhibit driver are a flip-flop output and a timing pulse from the inhibit pulse generator.

g. Pulse Generator. This circuit produces an output pulse whenever the logical input is true at a clock time. The pulse is used to control the other core memory circuits. Packaged two to a card.

h. Full Adder. This circuit accepts *one* digit from each of two registers plus a carry digit from the previous adder or the carry flip-flop. It produces a sum digit which may be used to set a flip-flop and a carry with its complement 'which can be used to set a flip-flop or drive the next adder. The carry delay is small enough to permit fifteen-bit addition in one AN/UYK-1 clock time. Two circuits are contained on one card.

i. Half Adder. This circuit accepts four digits from four consecutive bits of a register plus a carry digit from the previous half adder or the carry flip-flop. It produces four sum digits which can be used to set four flip-flops. A carry digit is also formed which is a function of the input carry digit and the four register digits formed. It can be used to set a flip-flop or drive the next half adder. The carry delay is small enough to permit fifteen bit counting in one AN/UYK-1 clock time. One four-bit half adder circuit is contained on one card.

j. Clock Generator. Consists of a transistorized oscillator and pulse shaping and amplifying circuits generating a 333 kc clock with 15 volts amplitude having pulses 0. 35 microsecond wide at half amplitude and 0. 1 microsecond rise time. Drives all flip-flops and other clocked elements. Packaged on two cards.

k. Transfer Logic Card. Contains 30 diodes and fifteen resistors in a configuration for effecting a complete fifteen-bit register transfer.

1. General Logical Circuitry. Logical gating structure for the AN/UYK-1 computer is "AND-AND-OR-OR", and uses only diodes and resistors. No change in the rules for logical structures is made from those in use for several years at Ramo-Wooldridge. Logic is packaged on the same size card as that used for active circuit elements.

4. 3 EQUIPMENT DESIGN

The following objectives are incorporated in the equipment design for the AN/UYK-1:

a. Environmental specifications suitable for Navy installations.

b. Performance reliability consistent with digital computer requirements.

c. Reasonable cost.

d. Human engineering practices which facilitate operation and maintenance.

e. Volume consistent with efficient packaging and consistent with Navy installations.

The AN-UYK-1 is approximately 59 inches high, 20 inches wide and 16 inches deep as shown in the Frontispiece. All computer components are fully accessible from the front. The power supply, memory unit, and blower are accessible by swinging the front section open. The computer will be operative in its open position.

The basic module for the computer circuitry is the etched circuit card. The dual flip-flop etched circuit card is shown in Figure 4-2.

Each card has a test point connector with contacts for a 0. 080 test probe and a right angle connector with 41 contacts for connecting to the socket in the main frame. Neon lights are mounted on flip-flop cards to indicate the state of these devices as an aid in maintenance. Standard etched wiring on only one side of the board provides for conventional dip soldering practices. Cards are mounted in groups of twenty-six on five-eighths centers. Figure 4-3 illustrates the insert mounting technique.

The control panel, mounted at the top of the cabinet, has two groups of controls, operator's controls and test and maintenance controls. Certain indicator lights are also mounted on the control panel. The AN/UYK-1 core planes will have a plastic coating over the grid as a protection from shock and vibration and will be mounted inside an insulated box which has the inside temperature thermostatically controlled at 55° C.

The cabinet will be designed and constructed to meet the requirements of its environment, including drop proofing and electrical protection. Louvers will provide for air flow. An extensive study will be made to design the supports for the assemblies inside of the cabinet to eliminate destructive resonances and to filter out the unacceptable shock and vibration from the susceptible components. The assistance of specialists in this field will result in an optimum design.

The thermally critical components in the proposed unit are the transistors, diodes, and core memory. The capacitors are not a problem

since the low temperature requirement is not stringent. With an upper temperature requirement of 50° C ambient, it is expected that forced air cooling and adequate heat sinks will be required to keep semiconductor junction temperatures within the reliable operating range. Fortunately, the standard practice of derating components to increase their reliability in computer circuits keeps their heat dissipation per unit surface area quite low.

5. SUMMARY OF AN/UYK-1 CHARACTERISTICS

Physical

Components - Solid State

Size - 16 inches deep; 20 inches wide, 59 inches high

Environmental Tolerance - General Requirement MIL-E- 16400C (Navy)
- Drop Proof MIL STD 108D
- Vibration MIL STD 167 (Ships)
- Shock MIL-S-901B (Navy)
- Temperature 0° - 50° C

Power - 115 volt, 60 or 400 cycle, 590 watts

Organization

Operation - Parallel by 15-bit word elements

Word Length - Variable in multiples of 15 bits, i.e., 15, 30, 45, etc.

Order Structure - Variable by stored logic to be single, double, triple or any address structure

Instruction Code - Adapted to the problem

Memory - 8, 192 word elements random access core
- 6 microsecond read-write cycle
- all operation times include memory access

Input-Output

Interrupt - 18 microseconds reaction time
- Interrupt subroutine
- Automatic return in 18 microseconds to prior task

Block Transfer - 18 microseconds setup time
- 12 microseconds per 15-bit word element

Available Transfers - 30-bit parallel
- 15-bit parallel

Internal

Typical Selected Instructions - Operation times include memory access times

		Operation Times (microseconds)	
		Add	Multiply
Single Address-Fixed Point-15 bit	Direct	**12**	**63**
	Interpretive	**30**	**93**
Triple Address-Fixed Point-30 bit		**72-150**	**348-486**
Triple Address-Floating Point-45 bit		**240-438**	**384-570**

Table Look-Up - 18 microseconds setup
- 12 microseconds per 15-bit word element

Match - 18 microseconds setup

- 12 microseconds per 15-bit word element

Branch or Skip - 12 or 18 microseconds

Block Transfer - 18 microseconds setup
- 12 microseconds per 15-bit word element